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PATENT & TRADEMARK OFFICE

DOCKET NO.: EIN-NL021330 (STNX01-21330) **PATENT**
CUSTOMER NO.: 84274

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	Edwin Rijpkema
Application No.	:	10/538,563
Filed	:	June 15, 2005
Title	:	COMBINED BEST EFFORT AND CONTENTION FREE GUARANTEED THROUGHPUT DATA SCHEDULING
Art Unit	:	2473
Examiner	:	Kao, Jutai
Confirmation No.	:	9446

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INFORMATION DISCLOSURE STATEMENT

Pursuant to the duty of disclosure under 37 C.F.R. § 1.56, Applicant submits this statement. This submittal is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure. The references herein are listed below and on the attached Forms PTO/SB/08A & B. Copies of the listed references are submitted herewith.

Foreign Patent No.	Country	Date
JP 2000-151703	Japan	May 30, 2000
JP 2000-295228	Japan	Oct. 20, 2000

Non-Patent References

Edwin Rijpkema, et al., "A Router Architecture for Networks on Silicon", Proceedings of Progress 2001, 2nd Workshop on Embedded Systems, pg. 1-8.

Mamoru Takajyo, et al., "Improvement for Packet Priority of the Packet Switch with Multiple Input Queues for Every Output Port", The Institute of Electronics, Information and Communication Engineers, Technical Report of IEICE SSE97-13, April 1997, 8 pages.

Translation of Office Action dated May 22, 2009 in connection with Japanese Patent Application No. 2004-561738.

Applicant hereby expressly reserves the right to swear behind the effective dates of any of the above Patents and to question the relevance and materiality of the Patents and Publications listed herein, in whole, in part, or in combination, subsequent to filing this Information Disclosure Statement.

Respectfully submitted,

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Date: 8/5/2010

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